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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,086	10/18/1999	WARREN M. FARNWORTH	98-0105.01	2322

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/420,086	Farnworth et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- Th MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 9, 2001*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *25-39 and 47-53* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *25-39 and 47-53* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *; 6 and*

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25-29, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (prior art-IDS, US Pat. 5783461) in view of Frankeny et al (US Pat. 5065227) and Pedder (US Pat. 5717245).

Regarding claims 25, 52 and 53, Hembree discloses a semiconductor component/package comprising:

- a composite substrate/interconnect (14/16 in Fig. 2) comprising a first surface with a conductive layer/trace (40, 56, 58, etc. in Fig. 2 and 4) and an opposing/second surface (31 in Fig. 2)
- a plurality of conductors on the conducting layer (68 in Fig. 2-5) on the first surface (Fig. 4 and 5; Col. 6, line 21), each conductor comprising a plurality of first grooves/raised contact members (40/68/70, etc. in Fig. 2-5A) through the conductive layer and configured for electrical connection with the semiconductor die

- a semiconductor die on the first surface in electrical communication with the conductors (die 12 in Fig. 2)

- a plurality of conductive lines/vias/second grooves through the substrate/interconnect (49 in Fig. 3A) from the first surface to the second surface and in electrical communication with the conductors (40 in Fig. 2), and

- a plurality of external contacts/balls on the second surface in electrical communication with the conductive vias (38 in Fig. 2; Col. 4, line 53)

(Fig. 2-5A; Col. 3, line 45- Col. 6, line 65).

Hembree fails to specify using a plurality of conductors defined by a plurality of laser machined grooves or vias through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer.

Pedder taches using conductive stubs/grooves/vias formed/trimmed by conventional laser trimming (Col. 2, line 25, Col. 8, line 38; Fig.2, and 9) on the conductive layer/trace of the substrate in a multichip module/ball grid package. Pedder further teaches forming conductive pattern comprising stubs/grooves (94 , 95, etc. in Fig. 9) using laser trimming/machining (Col. 8, line 45-54) which include conventional metallization/trace in first/X and second/Y directions.

Frankeny et al teach using conventional laser drilling/etching or punching of metal (Fig. 5; Col. 5, line 63- Col. 5, line 9) to expose the metal to define a plurality of vias (98 in Fig. 5) through the conductive layer (copper layer in Fig. 5). Frankeny et al further teach forming the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer where the conducting layer is patterned using conventional plating and etching methods. It would be obvious to one of ordinary skill in the art to use any of typical etching methods such as chemical/wet etch, laser-based, plasma etch etc. to form conductor pattern in first/X and second/Y directions.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of conductors defined by a plurality of laser machined first or second grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer laser machined grooves formed the conductive layer to improve the resonance characteristics and electrical performance of the contacts/device using Pedder and Frankeny et al's conductor structure in Hembree's component.

Regarding claims 26 and 27, Hembree discloses a semiconductor die flip chip bonded/mounted or wire bonded to the a plurality of bond pads on the conductors/substrate (56/60 in Fig. 4; Col. 6, line 21). Furthermore, Pedder teaches using a multichip module/ball grid package where the a

semiconductor chip or multichip can be mounted on the conductors using conventional wire bond or flip chip connections (Fig. 2; Col. 2, line 36; Col. 4, line 28; Col. 4, line 50).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of dice flip chip mounted or wire bonded to the conductors to achieve multichip connection capability using Pedder and Frankeny et al's's module design in Hembree's component.

Regarding claim 28, Hembree discloses a the substrate comprising a material selected from the group consisting of plastic, glass filled resin, silicon and ceramic (Col. 2, line 17-33; Col. 6, line 35).

Regarding claim 29, Hembree discloses external contacts comprising balls in a ball/grid array (Fig. 2-3A; Col. 4, line 48).

3. Claims 30-34, 47-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (prior art-IDS, US Pat. 5783461) in view of Frankeny et al (US Pat. 5065227) and Pedder (US Pat. 5717245).

Regarding claims 30-32, 47, 50 and 51, Hembree discloses a semiconductor component/package comprising:

- a composite substrate/interconnect (14/16 in Fig. 2) comprising a surface with a conductive layer/traces (40, 56 and 58 in Fig. 2 and 4) having a thickness
- a plurality of conductors having width and thickness (40, 56, 58 and 60 in Fig. 2, 4 and 5) on the first surface (Fig. 4 and 5; Col. 6, line 21), each conductor comprising grooves/raised contact members (40, 58, 60, 66, 68, etc. in Fig. 2, 4 and 5) through the conductive layer extending in a first and second directions (Fig. 2-5A; Col. 3, line 45- Col. 6, line 65), the conductor including a plurality of first pads/contacts (60 in Fig. 4-5A) on first ends
- a semiconductor die mounted on the substrate, the die comprising a plurality of second pads bonded (62 in Fig. 5A) to the first pads (Col. 6, line 25)
- a plurality of conductive lines/vias in the substrate/interconnect (49 in Fig. 3A) in electrical communication with the conductors (40 in Fig. 2), and
- a plurality of second/external contacts on the second surface in electrical communication with the conductive vias (38 in Fig. 2; Col. 4, line 53) and configured for an electrical connection to an external circuitry

(Fig. 2-5A; Col. 3, line 45- Col. 6, line 65).

Hembree fails to specify using a plurality of pairs of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated on either side by a pair of laser machined grooves.

As explained above for claim 25, Frankeny et al and Pedder teach forming the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer using conventional laser drilling or punching of metal.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of pairs of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated on either side by a pair of laser machined grooves to improve the electrical performance of the contacts/device using Frankeny et al and Pedder's laser drilled conductors in Hembree's semiconductor component.

Regarding claims 33, 48 and 49 as explained above for claims 26 and 27, Hembree further discloses a semiconductor die flip chip bonded/mounted or wire bonded to the a plurality of bond pads on the conductors/substrate (56/60 in Fig. 4; Col. 6, line 21).

Regarding claim 34, Hembree fails to specify using an encapsulant covering the die and a portion of the surface.

Peddler teaches using the conventional sealant/encapsulant to encapsulate the BGA package/module in the chip packaging art (Col. 1, line 55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to use an encapsulant covering the die and a portion of the surface to provide added protection in Hembree's semiconductor component.

4. Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (prior art-IDS, US Pat. 5783461) in view of Frankeny et al (US Pat. 5065227) and Pedder (US Pat. 5717245).

Regarding claims 35 and 37, as explained above for claims 25 and 30, Hembree fails to specify selecting the thickness of the conductive layer and width of the conductors to provide a selected impedance value for the conductors.

It is a matter of a design choice to select the conductor parameters such as thickness of the conducting layer, pitch/spacing or width of conductor/pad, material of the conductor, etc. in chip packaging and interconnection technology art to achieve the desired resistance, impedance, etc. for the interconnect/device. Pedder teaches using conductor/trace wiring design where the conventional wiring layout parameters such as spacing, pitch, number of conductors, vias, etc.

are selected to achieve the desired electrical performance related to electrical signal, power/ground, impedance and frequency requirements (Col. 5, line 11-Col. 6, line 50) for the multichip module/package.

Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate laser machined grooves formed through the conductive layer and the thickness of the conductive layer and width of the grooves being selected to provide an impedance value for the conductors to achieve the desired electrical performance using Pedder and Frankeny et al's design in Hembree's component.

Regarding claim 36, Hembree fails to specify using an encapsulant covering the die and a portion of the surface.

Peddler teaches using the conventional sealant/encapsulant to encapsulate the BGA package/module in the chip packaging art (Col. 1, line 55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to use an encapsulant covering the die and a portion of the surface to provide added protection in Hembree's semiconductor component.

Regarding claims 38 and 39, Hembree discloses a the substrate comprising a material selected from the group consisting of plastic, glass filled resin, ceramic or silicon having an electrically insulating layer on the surface (Col. 2, line 17-33; Col. 6, line 35).

Response to Arguments

5. Applicant's arguments filed on 10-09-01 have been fully considered but they are not persuasive.

A. Applicant contends that Frankeny et al or Pedder do not teach forming laser machined conductors.

However, as explained above for claim 25, Pedder teaches forming conductive pattern comprising stubs/grooves (94 , 95, etc. in Fig. 9) using laser trimming/machining (Col. 8, line 45-54) which include conventional metallization/trace in X/Y directions.

Frankeny et al teach using conventional laser drilling/etching or punching of metal (Fig. 5; Col. 5, line 63- Col. 5, line 9) to expose the metal define a plurality of vias (98 in Fig. 5) through the conductive layer (copper layer in Fig. 5). Frankeny et al further teach forming the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer where the conducting layer is patterned using conventional plating and etching methods. It would have been obvious to one of ordinary skill in the art to use any of typical etching methods such as chemical/wet etch, laser-based, plasma etch etc. to form conductor pattern in first/X and second/Y directions.

Furthermore, Applicant's claims 25, 30, 35, 47 and 52 do not distinguish over Hembree in view of Frankeny et al and Pedder regardless of the process for machining/etching grooves, because only the final product is relevant, not the process of making such as "laser machining or drilling". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

01-16-02

Tom Thomas

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